WHAT IS CLAIMED IS:

1. A delay transistor comprising:

a substrate;

a plurality of conduction channels embedded in the substrate;

a plurality of active regions embedded in the substrate, the active regions alternating with the conduction channels;

a source contact coupled with first alternating active regions;

a drain contact coupled with second alternating active regions; and

a gate structure overlaying the conduction channels, the gate structure being configured to receive an input signal, wherein the gate structure is a single gate structure, and wherein the gate structure provides an RC delay to the input signal and filters power and voltage spikes in the input signal, the RC delay being of a sufficiently long duration so as to decrease the switching speed of the transistor and allow the gate structure to filter power and voltage spikes.

2. The delay transistor of claim 1 wherein the gate structure has a serpentine shape.

3. The delay transistor of claim 1 wherein the gate structure comprises polysilicon.

4. The delay transistor of claim 1 wherein the delay transistor further comprises a plurality of diodes coupled with the single gate structure, the diodes being reversed biased, wherein the diodes contribute additional capacitance to the RC delay.

5. The trimming circuit of claim 1 wherein the delay transistor is an NMOS transistor.

6. The trimming circuit of claim 1 wherein the delay transistor is a PMOS transistor.

7. A delay transistor comprising:

a plurality of transistors coupled in parallel, each transistor being coupled between a first voltage potential and a second voltage potential; and

a plurality of diodes coupled between the gates of the transistors and the second voltage potential, the gates being formed by a single gate structure, wherein the combination of the gate and the diodes provide a distributed RC delay to the input signal and filters power and voltage spikes in the input signal, the RC delay being of a sufficiently long duration so as to decrease the switching speed of the transistor and allow the gate structure to filter power and voltage spikes.

8. A delay pad structure comprising:

a substrate;

an active region embedded in the substrate, and active region being configured to receive an input signal, the active region having a serpentine shape, the active region providing an RC delay to the input signal and filtering power and voltage spikes in the input signal; and

a plurality of diodes coupled with the active region, the diodes being reversed biased, wherein the diodes provide additional capacitance to the RC delay.

9. The delay pad structure of claim 8 wherein the substrate is a p-type substrate.

10. The delay pad structure of claim 8 wherein the active region is an n+ region.

11. The delay pad structure of claim 8 wherein the delay pad structure is used in a trimming circuit for modifying electronic circuits.

12. A delay line structure comprising:

a substrate;

a thin oxide layer coupled onto a first side of the substrate, the thin oxide layer having a square shape;

a polysilicon layer coupled onto the thin oxide layer, the polysilicon layer being configured to receive an input signal, the combination of the thin oxide layer coupled between the substrate and the polysilicon layer providing an RC delay to the input signal and filtering power and voltage spikes in the input signal; and

a plurality of diodes coupled with the polysilicon layer, the diodes being reversed biased, wherein the diodes provide additional capacitance to the RC delay.

13. The delay line structure of claim 12 wherein the substrate is a p-type substrate.

14. The delay pad structure of claim 12 wherein the delay pad structure is used in a trimming circuit for modifying electronic circuits.